

FORM PTO-1449 (modified) To: U.S. Department of Commerce (PW FORM PAT-1449) Patent and Trademark Office				Atty. Dkt. No.	Mr. [REDACTED] [REDACTED] [REDACTED]	Client Ref. [REDACTED] [REDACTED]				
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT										
Date: June 24, 2003		Page 1 of 1	Applicant: MATSUDA et al.							
			Appln. No.: UNASSIGNED							
			Filing Date: June 24, 2003							
			Examiner: D. LE		Group Art Unit: 2818					
U.S. PATENT DOCUMENTS										
Examiner's Initials*	Document Number	Date MM/YYYY	Name (Family Name of First Inventor)		Class	Sub Class	Filing Date (if appropriate)			
DK	AR 6,319,807	11/2001	Yeh et al.							
DK	BR 6,353,249	03/2002	Boyd et al.							
DK	CR 5,856,225	01/1999	Lee et al.							
DK	DR 6,087,208	07/2000	Krivokapic et al.							
ER										
FR										
GR										
HR										
IR										
JR										
KR										
LR										
MR										
NR										
FOREIGN PATENT DOCUMENTS							English Abstract		Translation Readily Available	
	Document Number	Date MM/YYYY	Country	Inventor Name			Enclosed	No	Enclose	No
	OR									
	PR									
	QR									
	RR									
	SR									
	TR									
	UR									
OTHER (including in this order: Author, Title, Periodical Name, Date, Pertinent Pages, etc.)										
DK	VR	A. Chatterjee et al., "Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process," IEDM, 1997, pp. 821-824								
DK	WR	A. Chatterjee et al., "CMOS Metal Replacement Gate Transistors Using Tantalum Pentoxide Gate Insulator," IEDM, 1998, pp. 777-780								
DK	XR	Yagishita et al., "High Performance Metal Gate MOSFETs Fabricated by CMP for 0.1um Regime," IEDM 1998, pp. 785-788								
	YR									
	ZR									
	AAR									
Examiner <i>John Doe</i>				Date Considered: <i>6/08/04</i>						
*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.										